IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	
Guy L. STEELE, Jr.	Group Art Unit: 2193
Application No.: 10/035,587	Examiner: Mai, Tan V.
Filed: December 28, 2001	
For: FLOATING POINT STATUS INFORMATION ACCUMULATION CIRCUIT	Confirmation No.: 2874

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Sir:

APPEAL BRIEF UNDER BOARD RULE § 41.37

In support of the Notice of Appeal filed September 30, 2005, and further to Board Rule 41.37, Appellant presents this brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 1.17(c).

This Appeal Brief is being filed concurrently with a Petition for an Extension of Time for four months and the appropriate fee.

This Appeal responds to the Notice of Panel Decision from Pre-Appeal Brief Review mailed on November 7, 2005 and the Final Office Action mailed on June 3, 2005, which rejected claims 1-3 and 5-47 under 35 U.S.C. § 103(a).

If any additional fees are required or if the enclosed payment is insufficient, Appellant requests that the required fees be charged to Deposit Account No. 06-0916.

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I. REAL PARTY IN INTEREST

Sun Microsystems, Inc. is the real party in interest, as indicated by the assignment in its name, recorded at Reel 012440, Frame 0787 on December 28, 2001.

II. RELATED APPEALS AND INTERFERENCES

In accordance with 37 C.F.R. § 41.37(c)(1)(ii), Appellant advises the Board of Patent Appeals and Interferences (the "Board") of the following pending appeals, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the instant appeal:

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,595, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,584, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,579, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,647, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,580, in which an Appeal Brief was filed concurrently herewith.

III. STATUS OF CLAIMS

Claims 1-47 remain pending and under current examination.

Claims 1-3 and 5-47 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,995,991 to Huang et al. ("*Huang*"); and claims 1-3 and 5-47 have been finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,009,511 to Lynch et al. ("*Lynch*"). Appellant appeals these rejections. The attached Appendix contains a clean copy of the claims involved in the appeal, claims 1-47.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendments under 37 C.F.R. § 1.116 have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1, 18, and 33 of this application recite a system, method, and computer-readable medium for performing floating point operations. *Specification*, p. 1, paragraph 002.

Digital electronic devices, such as digital computers, calculators and other devices, perform arithmetic calculations on values in integer, or "fixed point," format, in fractional, or "floating point" format, or both. *Specification*, p. 1, paragraph 003. Institute of Electrical and Electronic Engineers (IEEE) Standard 754, (hereinafter "IEEE Std. 754") published in 1985 and adopted by the American National Standards Institute (ANSI), defines several standard formats for expressing values in floating point format and a number of aspects regarding behavior of computation in connection therewith. *Id.*

In prior art devices that perform floating point computations, floating point status information generated by the computation is stored in a floating point status register. *Id.* at p. 8, paragraph 019. The status information is stored as conditions, represented by flags that are stored in the floating point status register. *Id.* at p. 8, paragraph 025.

However, the modes (*e.g.*, the rounding modes and traps enabled/disabled mode), flags (*e.g.*, flags representing the status information), and traps that are required to implement IEEE Std. 754 introduce implicit serialization issues. *Id.* at p. 9, paragraph 027. Implicit serialization is essentially the need for serial control of access (read/write) to and from globally used registers, such as a floating point status register. *Id.* The potential for implicit serialization makes the Standard difficult to implement coherently and efficiently in today's superscalar and parallel processing architectures without loss of performance. *Id.* at pp. 10, paragraph 027.

Moreover, the implicit side effects of a procedure that can change the flags or modes can make it very difficult for compilers to perform optimizations on floating point code. *Id.* at p. 10, paragraph 028. As a result, compilers for most languages usually assume that every procedure call is an optimization barrier in order to be safe. *Id.*

The claimed invention addresses these and other problems of prior art floating point computational systems. *Id.* at p. 11, paragraph 034. Since the floating point status information is part of the floating point representation of the result, instead of being separate and apart from the result, there is no need to access external circuitry (e.g., floating point status register). *Id.* at p. 15, paragraph 047. Thus, the implicit serialization that is required by maintaining the floating point status information separate and apart from the result may be obviated. *Id.*

The invention, as recited by independent claim 1, relates to a flag combining circuit (FIG. 1). *Id.* at pp. 11-12, paragraph 035. The circuit may include an analysis circuit (FIG. 1, 12A) that receives a plurality of operands each of which having encoded status flag information, the analysis circuit being operative to analyze the plurality of operands and to provide an indication of one or more predetermined formats (FIG. 2) in which the plurality of operands are represented. *Id.* The flag combining circuit may also include a result assembler (FIG. 1, 14) that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands. *Id.* at p. 12, paragraphs 0036-0037; pp. 24-25, paragraph 0098.

The invention, as recited by independent claim 18, relates to a method for combining flag information. *Id.* at p. 12, paragraph 0038. The method may include receiving a plurality of operands, each of which having encoded status flag information and analyzing, using an accumulation circuit (FIG. 1, 10), the plurality of operands to provide indications of one or more predetermined formats (FIG. 2) in which the plurality of operands are represented. *Id.* pp. 14-15, paragraphs 0046-0047. The method may also include generating control signals based on the indications of the one or more predetermined formats. *Id.* at p. 12, paragraph 0038. Further, the method may include assembling an accumulated result based at least upon the generated control signals and input signals, the accumulated result representing a value and combining the encoded status flag information from each of the plurality of operands. *Id.*

The invention, as recited by independent claim 33, relates to a computer-readable medium on which is stored a set of instructions for combining operands, which

when executed perform steps. *Id.* at p. 39, paragraph 00159-00160. The steps may include receiving a plurality of operands, each of which having encoded status flag information and analyzing the plurality of operands to provide indications of one or more predetermined formats (FIG. 2) in which the plurality of operands are represented. *Id.* pp. 14-15, paragraphs 0046-0047. The steps may also include generating control signals based on the indications of the one or more predetermined formats. *Id.* at p. 12, paragraph 0038. Further, the steps may include assembling an accumulated result based at least upon the generated control signals and input signals, the accumulated result representing a value and combining the encoded status flag information from each of the plurality of operands. *Id.*

VI. GROUNDS OF REJECTION TO BE REVIEWED

A. Claims 1-3 and 5-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,995,991 to Huang et al. ("*Huang*"). *See Final Office Action mailed June 3, 2005*, p. 2.

B. Claims 1-3 and 5-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,009,511 to Lynch et al. ("*Lynch*"). *See Final Office Action mailed June 3, 2005*, p. 2.

VII. ARGUMENT

A. Introduction

In view of the following arguments, Appellant respectfully requests the Board to reverse the Examiner's rejection of claims 1-3 and 5-47 under 35 U.S.C. § 103(a).

Several basic factual inquires must be made in order to determine the obviousness or non-obviousness of claims of a patent application under 35 U.S.C. § 103. These factual inquiries, set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), require the Examiner to:

> (1) Determine the scope and content of the prior art;
> (2) Ascertain the differences between the prior art and the claims in issue;
> (3) Resolve the level of ordinary skill in the pertinent art; and
> (4) Evaluate evidence of secondary considerations.

The obviousness or nonobviousness of the claimed invention is then evaluated in view of the results of these inquiries. *Graham*, 383 U.S. at 17-18, 148 USPQ 467.

Thus, in order to carry the initial burden of establishing a *prima facie* case of obviousness that satisfies the *Graham* standard, the Examiner must show that the prior art reference teaches or suggests all the claim elements. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The Examiner must also show that there is some suggestion or motivation, either in the reference or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). "Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 1998) (citations omitted). In addition, the suggestion or motivation "must be found in the prior art reference, not in the Applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

B. The rejection of claims 1-3 and 5-47 under 35 U.S.C. § 103(a) as being unpatentable over *Huang*

1. Claims 1-3 and 5-47 patentably distinguish from *Huang*

Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example, "an analysis circuit that receives a plurality of operands each of which having encoded status flag information, the analysis circuit being operative to analyze the plurality of operands and to provide an indication of one or more predetermined formats in which the plurality of operands are represented" (emphasis added).

The Examiner concedes that *Huang* fails to teach or suggest this element, stating "Huang et al. do not specifically detail the claimed 'analyzer circuit that receives a plurality of operands each of which having **encoded status flag** information" (emphasis in original, *Office Action mailed October 22, 2004* at p. 3). However, the Examiner has not provided any reference to supplement *Huang* by teaching or suggesting this element, despite Appellant's requests. *See Amendment filed February 2, 2005* at pp. 15-16; *Request for Reconsideration filed August 3, 2005* at p. 3.

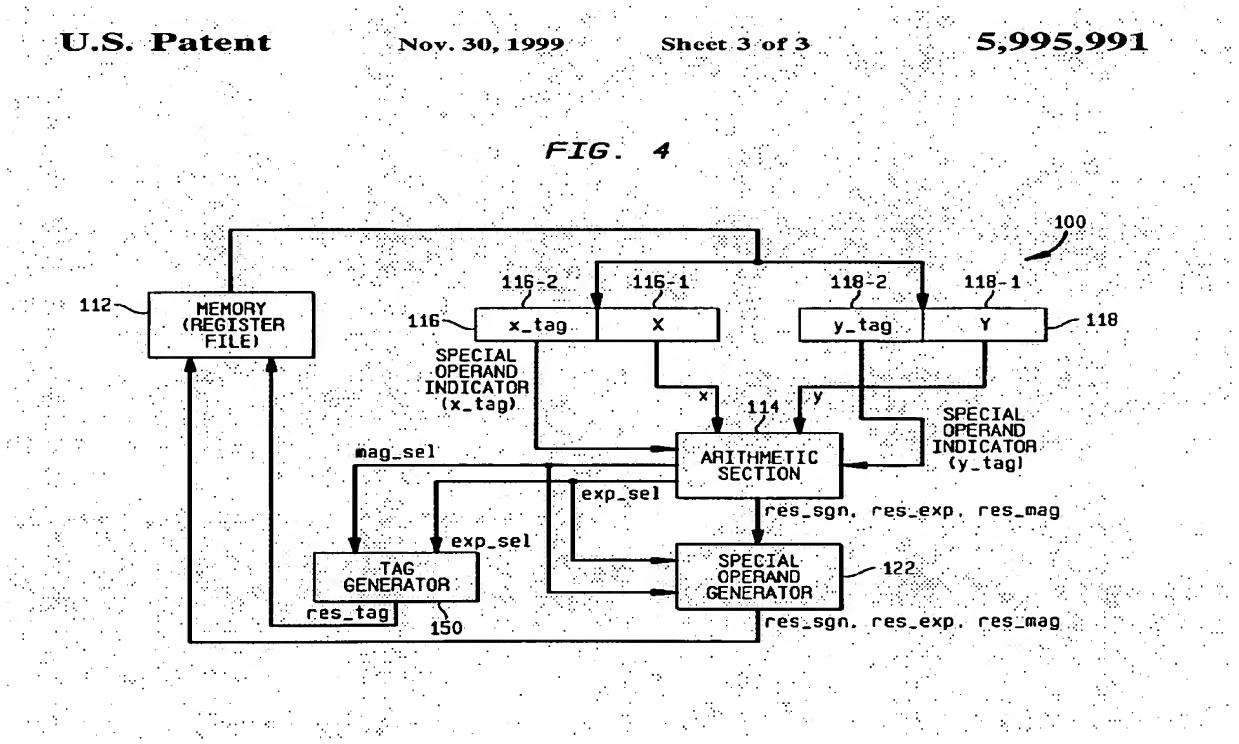
In an attempt to cure this deficiency of *Huang*, the Examiner asserts "[h]owever, Huang et al do disclose X and Y operand registers each includes [sic] a special operand indicator" (emphasis added, *Office Action mailed October 22, 2004* at p. 3). The Examiner's assertion fails to cure the deficiencies of *Huang*.

First, the Examiner has not identified specific teachings in *Huang* which correspond to the Examiner's coined term "special operand indicator." The Examiner has also not explained how this term relates to, for example, the claimed "plurality of

operands each of which having encoded status flag information" as recited by claim 1 (emphasis added).

Second, even assuming the Examiner's coined term "special operand indicator" refers to a tag value of *Huang* (*Huang*, FIG. 4, 116-2), *Huang's* teaching of a "tag value" does not constitute a teaching or suggestion of a "plurality of operands each of which having encoded status flag information" (emphasis added) as recited by claim 1.

Huang specifically contradicts that a "tag value" is "encoded" in an "operand," as recited by claim 1. *Huang* teaches "each portion of the registers 116 and 118 has an operand value storage portion 116-1 and 118-1 and a tag value storage portion 116-2 and 118-2" (emphasis added, *Huang*, col. 6, line 66 through col. 7, line 2). As illustrated in Fig. 4 of *Huang*, which Appellant reproduces below, *Huang* thus teaches a separate operand value storage portion, 116-1, and a separate tag value storage portion for the x_tag 116-2 (*Huang*, col. 6, line 66 through col. 7, line 2; Fig. 4).



Huang's tag value (possibly corresponding to status flag information) stored in 116-2 is clearly not "encoded" within *Huang's* operand value stored in 116-1. Therefore, *Huang* does not teach or suggest at least a "plurality of operands each of which having encoded status flag information," as recited by claim 1 (emphasis added).

Moreover, independent claim 1 recites a combination also including, for example, "a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands" (emphasis added). *Huang* does not teach or suggest at least this additional element. The Examiner has not identified any portions of *Huang* which provide a teaching or suggestion of a "result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands," as recited by claim 1 (emphasis added). *See Office Action mailed October 22, 2004* at pp. 3-4. For at least this reason, the Examiner's rejection is improper.

Structures such as those taught by *Huang* were acknowledged in the Background section of Appellant's specification, which states "conditions are typically represented by flags that are stored in the floating point status register separate from the result itself" (paragraph 025). Claim 1 specifically distinguishes over such structures, calling for a "plurality of operands each of which having encoded status flag information" (emphasis added).

Because *Huang* does not teach or suggest each and every element recited by claim 1, no *prima facie* case of obviousness has been established for this claim.

Moreover, there is no motivation or suggestion to modify *Huang* to arrive at Appellant's claimed invention. The Examiner relies on a single reference, *Huang*, in rejecting claims 1-3 and 5-47. Even where the Examiner relies on a single reference, there still "must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 1998) (citations omitted).

The Examiner asserts that it "would have been obvious ... to design the claimed invention according to Huang et al's teachings because the device is an **arithmetic calculation circuit (100)** having **special operand indicator** in each operand register." *Office Action mailed October 22, 2004* at p. 4 (emphasis in original). This unsupported assertion by the Examiner fails to meet the requisite high threshold of an objective indication that one of skill in the art would modify *Huang* to arrive at Appellant's claimed invention. Merely asserting that a device is an "arithmetic calculation unit" does not constitute motivation to modify *Huang* to arrive at Appellant's claimed invention.

First, the Examiner's assertion is directed to a special operand indicator "in each operand register." *Id.* (emphasis added). Discussion of "a special operand indicator in a each operand register," however, does not constitute motivation for a "plurality of operands each of which having encoded status flag information," as recited by claim 1 (emphasis added). Discussion of "a special operand indicator in a each operand register," also does not constitute motivation for a "result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands," as recited by claim 1 (emphasis added).

Second, the Examiner uses impermissible hindsight in reconstructing Appellant's claimed invention. A determination of obviousness must "take into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and ... [must] not include knowledge gleaned only from" Appellant's disclosure. *In re McLaughlin*, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971) (emphasis added). As discussed above, the Examiner concedes that *Huang* does not teach determining a "plurality of operands each of which having encoded status flag information." *Office Action mailed October 22, 2004* at p. 3. No other reference is cited to cure this deficiency. Therefore, the Examiner's determination of obviousness could not have been founded on knowledge within the level of skill in the art when Appellant's claimed invention was made. Such determination instead impermissibly relied on hindsight reasoning by looking to Appellant's specification. For at least this additional reason, there is no motivation to modify *Huang* to arrive at Appellant's invention as recited by claim 1.

Accordingly, there is no motivation to modify *Huang* to arrive at Appellant's invention recited by claim 1. Therefore, no *prima facia* case of obviousness has been established for claim 1 for at least this additional reason.

Independent claims 18 and 33, although of different scope, recite elements similar to those recited by claim 1. Claims 2, 3, 5-17, 19-32, and 34-47 depend from independent claims 1, 18, and 33 and therefore include all of the elements recited therein. Accordingly, no *prima facie* case of obviousness has been established with respect to claims 2, 3, and 5-47 for at least the reasons discussed above regarding claim 1. Appellant requests the Board to overturn the rejection of claims 1-3 and 5-47.

2. Claims 3, 5-17, 20-32, and 35-47 patentably distinguish from *Huang*

Huang does not disclose each and every element of dependent claims 3, 5-17, 20-32, and 35-47. In fact, the Examiner has not addressed any of the elements recited by dependent claims 3, 5-17, 20-32, and 35-47, other than to say that these features are "well known" and "obvious." *See Office Action mailed October 22, 2004* at p. 4. These bare assertions fail to meet the requirement that the prior art teach or suggest each and every element of claims 3, 5-17, 20-32, and 35-47. Moreover, the Examiner has not provided any motivation to make the alleged design choice modification. *Id.*

Because the Examiner has shown neither a teaching or suggestion in the prior art of each and every claim element, nor the requisite motivation to modify *Huang* to arrive at Appellant's claimed invention, no *prima facie* case of obviousness has been established with respect to claims 3, 5-17, 20-32, and 35-47. Appellant requests that the Board overturn the Examiner's rejection.

C. The rejection of claims 1-3 and 5-47 under 35 U.S.C. § 103(a) as being unpatentable over *Lynch*

1. Claims 1-3 and 5-47 patentably distinguish from *Lynch*

The Examiner's rejections contain clear errors and omit essential elements necessary to establish a *prima facie* case of obviousness for Appellant's claims 1-3 and 5-47 based on *Lynch*.

Independent claim 1 recites a combination including, for example, "an analysis circuit that receives a plurality of operands each of which having encoded status flag information, the analysis circuit being operative to analyze the plurality of operands and

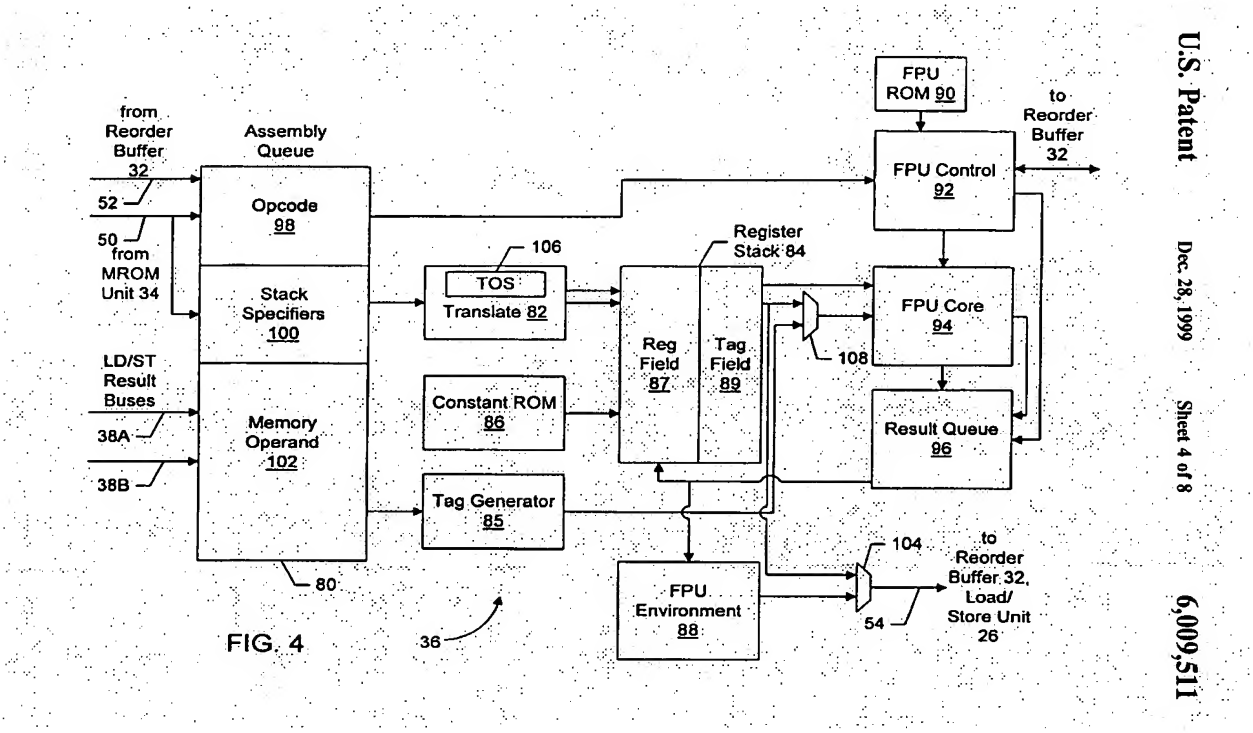
to provide an indication of one or more predetermined formats in which the plurality of operands are represented" (emphasis added).

Once again, the Examiner concedes that the cited reference fails to teach or suggest this element, stating "Lynch et al. do not specifically detail the claimed 'analyzer circuit that receives a plurality of operands each of which having **encoded status flag** information" *Office Action mailed October 22, 2004* at p. 5 (emphasis in original). However, the Examiner has not cited any additional reference to cure this admitted deficiency of *Lynch*, despite Appellant's requests. *See Amendment filed February 18, 2005* at pp. 17-18; *Request for Reconsideration filed August 3, 2005* at pp. 10-11.

Instead, the Examiner attempts to cure the deficiency by asserting "[h]owever, Lynch et al do disclose the ... appending tag values to each floating point number, the floating point unit can quickly determine which floating point numbers are special floating point numbers and the type of special floating point number." *Office Action mailed June 3, 2005* at p. 5. The Examiner appears to assert that *Lynch's* element 84 (Fig. 4) constitutes an "operand" which contains tag field 89 (alleged status). *See Office Action mailed October 22, 2004* at p. 5. This is not correct.

First, the Examiner has not explained how *Lynch's* "tag values" relate to, for example, "a plurality of operands each of which having encoded status flag information," as recited by claim 1. Even if *Lynch's* tag value were to constitute the claimed "status," (which Appellant does not concede) the tag value of *Lynch* is not "encoded" within each operand, as recited by claim 1.

Fig. 4 of *Lynch*, which Appellant reproduces below, clearly illustrates that Tag Field 89 (alleged status) and Reg Field 87 (operand) are separate from each other and are stored within register stack 84.



Moreover, *Lynch* specifically states that element 84 is a register stack, not an operand. *Lynch* also states that register stack 84 contains a Reg Field 87 for storing an operand separate from a Tag Field 89 for storing a tag (alleged status). *See Lynch*, col. 15, lines 63-67. "Separate from" cannot constitute "encoded" within the operand, as recited by claim 1.

Moreover, independent claim 1 recites a combination including, for example, "a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands" (emphasis added). The Examiner has not addressed this element or identified any specific teachings of *Lynch* which

would allegedly teach or suggest "a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands," as recited by independent claim 1. *See Office Action mailed October 22, 2004* at p. 5. For at least this reason, the Examiner's rejection is improper.

As with the structures of *Huang*, discussed above, structures such as those taught by *Lynch* were acknowledged in the Background section of Appellant's specification, which states "conditions are typically represented by flags that are stored in the floating point status register" (paragraph 025). Claim 1 specifically distinguishes over such structures, calling for "a plurality of operands each of which having encoded status flag information" (emphasis added).

Because the *Lynch* does not teach or suggest each and every element recited by claim 1, no *prima facie* case of obviousness has been established with respect to claim 1.

Further, the Examiner has not identified any motivation or suggestion to modify *Lynch*, the sole cited reference, to arrive at Appellant's claimed invention. Instead, the Examiner merely asserts that "it would have been obvious to ... design the claimed invention according to Lynch et al's teachings because the device is a **floating point unit (36)** having the 'determine which floating point numbers are special floating point numbers and the type of special floating point number' as claimed" (*Office Action mailed October 22, 2004* at p. 6, emphasis in original). This unsupported assertion by the Examiner fails to meet the requisite high threshold of an objective indication that one of skill in the art would modify *Lynch* to arrive at Appellant's claimed invention. Merely

asserting that a device is a "floating point unit" does not constitute motivation to modify *Lynch* to arrive at Appellant's claimed invention.

First, the Examiner's assertion is directed to determining "which floating point numbers are special floating point numbers and the type of special floating point number" (*Office Action mailed October 22, 2004* at p. 5). However, such discussion of generally determining "which numbers are special floating point numbers" does not constitute motivation for "a plurality of operands each of which having encoded status flag information," as recited by claim 1 (emphasis added). The discussion of generally determining "which numbers are special floating point numbers" also does not constitute motivation for "a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands," as recited by claim 1 (emphasis added).

Second, *Lynch's* teaching that "a tag value is appended to each floating point number stored in a floating point register" (*Lynch*, col. 5, lines 44-45) directly teaches away from the claimed structure, which requires "a plurality of operands each of which having encoded status flag information" (emphasis added).

Finally, the Examiner again uses impermissible hindsight in reconstructing Appellant's claimed invention. As discussed above, the Examiner concedes that *Lynch* does not teach "a plurality of operands each of which having encoded status information." *Office Action mailed October 22, 2004* at p. 5 (emphasis removed). No other reference is cited to cure this deficiency. Therefore, the Examiner's determination of obviousness could not have been founded on knowledge within the level of skill in the

art when Appellant's claimed invention was made. Such determination instead impermissibly relied on hindsight reasoning by looking to Appellant's specification. For at least this additional reason, there is no motivation to modify *Lynch* to arrive at Appellant's invention as recited by claim 1.

Because there is no motivation to modify *Lynch* to arrive at Appellant's invention recited by claim 1, no *prima facia* case of obviousness has been established, at least for this additional reason.

Independent claims 18 and 33, although of different scope, recite elements similar to those recited by claim 1. Claims 2, 3, 5-17, 19-32, and 34-47 depend from independent claims 1, 18, and 33 and therefore include all of the elements recited therein. Accordingly, no *prima facie* case of obviousness has been established with respect to claims 2, 3, and 5-47 for at least the reasons discussed above regarding claim 1. Appellant requests the Board to overturn the Examiner's rejection.

2. Claims 3, 5-17, 20-32, and 35-47 patentably distinguish from *Lynch*

Lynch does not disclose each and every element of dependent claims 3, 5-17, 20-32, and 35-47. As with *Huang*, discussed above, the Examiner has not addressed any of the elements recited by dependent claims 3, 5-17, 20-32, and 35-47, other than to say that "[t]hese features are obvious" and "well known." *See Office Action mailed October 22, 2004* at p. 5. This bare assertion meets neither the requirement for showing how *Lynch* allegedly teaches or suggests each and every element of dependent claims 3, 5-17, 20-32, and 35-47, nor the requirement to establish motivation to make the alleged modification. *Id.* Accordingly, no *prima facie* case of obviousness

has been established with respect to claims 3, 5-17, 20-32, and 35-47. Appellant requests that the Board overturn the Examiner's rejection.

D. Summary

The Examiner has not established a *prima facie* case of obviousness with respect to the presently appealed claims. In particular, the references cited by the Examiner in the appealed rejections do not teach or suggest all of the claim limitations. Furthermore, there is no suggestion or motivation, either in the cited references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine references, and the references, in fact, teach away from the claimed structure. *See* M.P.E.P. § 2143. Thus, the Examiner has failed to meet the criteria required for a *prima facie* showing of obviousness.

VIII. CONCLUSION

For the reasons given above, pending claims 1-47 are allowable and reversal of the Examiner's rejections are respectfully requested.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 7, 2006

By: _____
Nathan A. Sloan
Reg. No. 56,249

IX. Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

1. A flag combining circuit, comprising:

an analysis circuit that receives a plurality of operands each of which having encoded status flag information, the analysis circuit being operative to analyze the plurality of operands and to provide an indication of one or more predetermined formats in which the plurality of operands are represented; and

a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands.

2. The flag combining circuit of claim 1, wherein at least one of the plurality of operands is a floating point operand.

3. The flag combining circuit of claim 1, further comprising one or more operand buffers that receive the plurality of operands and transfers them to the analysis circuit.

4. The flag combining circuit of claim 1, further comprising a decision circuit that receives the indication from the analysis circuit and provides a second indication to the result assembler.

5. The flag combining circuit of claim 1, wherein the predetermined formats represent a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

6. The flag combining circuit of claim 1, wherein encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag.

7. The flag combining circuit of claim 5, wherein the overflow format represents one of a +OV status and a -OV status.

8. The flag combining circuit of claim 7, wherein the overflow format includes a set inexact status flag.

9. The flag combining circuit of claim 5, wherein the underflow format represents one of a +UN status and a -UN status.

10. The flag combining circuit of claim 9, wherein the underflow format includes a set inexact status flag.

11. The flag combining circuit of claim 5, wherein a least significant bit in the plurality of operands represents a set inexact status flag.

12. The flag combining circuit of claim 1, wherein the accumulated result produced is assembled using one of a commutative and an associative flag-combining operation.

13. The flag combining circuit of claim 1, wherein the accumulated result produced is in a NaN format.

14. The flag combining circuit of claim 13, wherein at least one of the plurality of operands is in the NaN format.

15. The flag combining circuit of claim 1, wherein the accumulated result represents information from one of the plurality of operands that has a larger fraction field.

16. The flag combining circuit of claim 1, wherein a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands.

17. The flag combining circuit of claim 1, wherein the result assembler produces the accumulated result in a NaN formatted one of the plurality of operands.

18. A method for combining flag information, comprising the steps of:

receiving a plurality of operands, each of which having encoded status flag information;

analyzing, using an accumulation circuit, the plurality of operands to provide indications of one or more predetermined formats in which the plurality of operands are represented;

generating control signals based on the indications of the one or more predetermined formats; and

assembling an accumulated result based at least upon the generated control signals and input signals, the accumulated result representing a value and combining the encoded status flag information from each of the plurality of operands.

19. The method of claim 18, wherein receiving the plurality of operands includes receiving at least one floating point operand.

20. The method of claim 18, wherein analyzing the plurality of operands includes providing an indication of predetermined formats representing a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

21. The method of claim 18, wherein encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag.

22. The method of claim 20, wherein the overflow format represents one of a +OV status and a -OV status.

23. The method of claim 22, wherein the overflow format includes a set inexact status flag.

24. The method of claim 20, wherein the underflow format represents one of a +UN status and a -UN status.

25. The method of claim 24, wherein the underflow format includes a set inexact status flag.

26. The method of claim 18, wherein assembling the accumulated result includes using one of a commutative and an associative flag-combining operation.

27. The method of claim 18, wherein assembling the accumulated result produces a result in a not-a-number (NaN) format.

28. The method of claim 27, wherein at least one of the plurality of operands is in the NaN format.

29. The method of claim 18, wherein assembling the accumulated result includes using at least two of the plurality of operands in a NaN format.

30. The method of claim 29, wherein assembling the accumulated result includes representing information from which of the at least two of the plurality of operands has a larger fraction field.

31. The method of claim 18, wherein a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands.

32. The method of claim 18, wherein assembling the accumulated result includes producing the accumulated result in a NaN formatted one of the plurality of operands.

33. A computer-readable medium on which is stored a set of instructions for combining operands, which when executed perform steps comprising:

receiving a plurality of operands, each of which having encoded status flag information;

analyzing the plurality of operands to provide indications of one or more predetermined formats in which the plurality of operands are represented;

generating control signals based on the indications of the one or more predetermined formats; and

assembling an accumulated result based at least upon the generated control signals and input signals, the accumulated result representing a value and combining the encoded status flag information from each of the plurality of operands.

34. The computer-readable medium of claim 33, wherein receiving the plurality of operands includes receiving at least one floating point operand.

35. The computer-readable medium of claim 33, wherein analyzing the plurality of operands includes providing an indication of predetermined formats representing a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

36. The computer-readable medium of claim 33, wherein encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag.

37. The computer-readable medium of claim 35, wherein the overflow format represents one of a +OV status and a -OV status.

38. The computer-readable medium of claim 37, wherein the overflow format includes a set inexact status flag.

39. The computer-readable medium of claim 35, wherein the underflow format represents one of a +UN status and a -UN status.

40. The computer-readable medium of claim 39, wherein the underflow format includes a set inexact status flag.

41. The computer-readable medium of claim 33, wherein assembling the accumulated result includes using one of a commutative and an associative flag-combining operation.

42. The computer-readable medium of claim 33, wherein assembling the accumulated result produces a result in a not-a-number (NaN) format.

43. The computer-readable medium of claim 42, wherein at least one of the plurality of operands is in the NaN format.

44. The computer-readable medium of claim 33, wherein assembling the accumulated result includes using at least two of the plurality of operands in a NaN format.

45. The computer-readable medium of claim 44, wherein assembling the accumulated result includes representing information from which of the at least two of the plurality of operands has a larger fraction field.

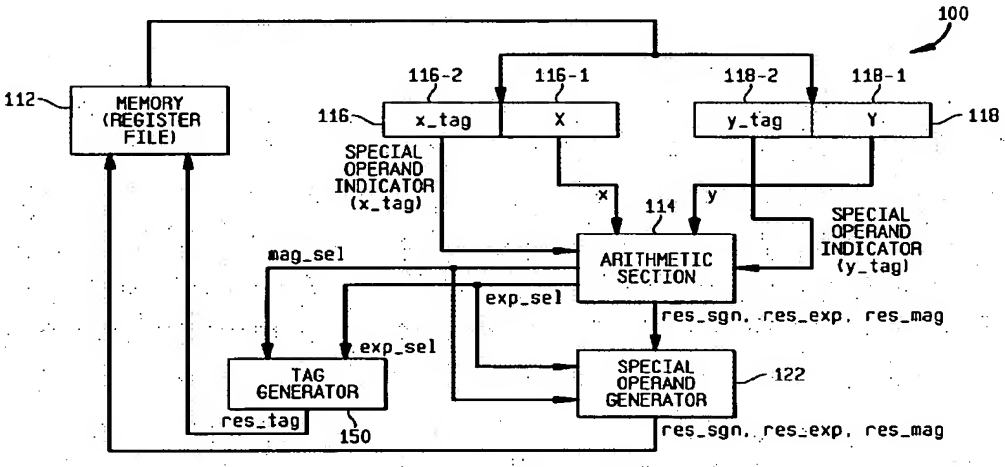
46. The computer-readable medium of claim 33, wherein a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands.

47. The computer-readable medium of claim 33, wherein assembling the accumulated result includes producing the accumulated result in a NaN formatted one of the plurality of operands.

X. Evidence Appendix to Appeal Brief Under Rule 41.37(c)(1)(ix)

Appellant relies on Fig. 4 of *Huang* and on Fig. 4 of *Lynch*, both of which are reproduced below.

FIG. 4



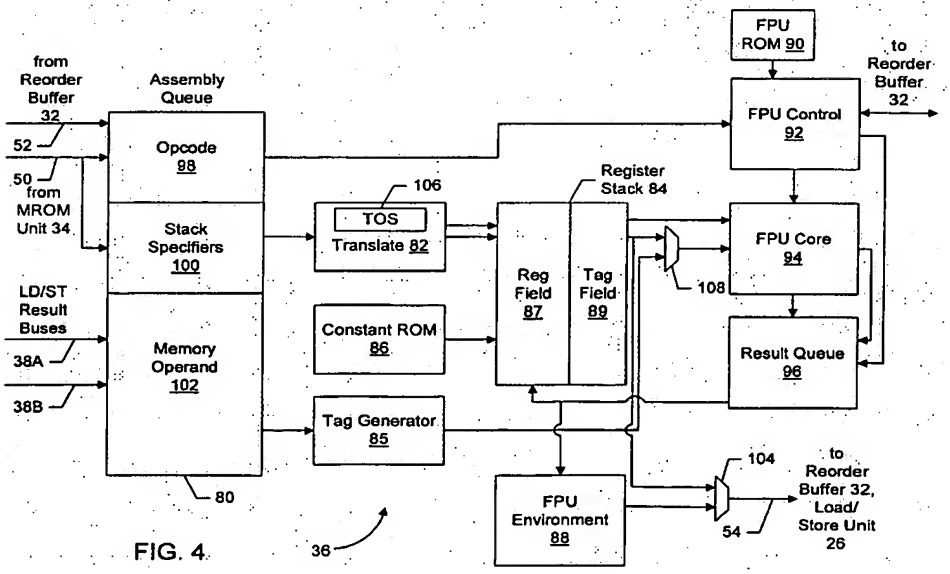


FIG. 4

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XI. Related Proceedings Appendix to Appeal Brief Under Rule 41.37(c)(1)(x)

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,595, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,584, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,579, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,647, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,580, in which an Appeal Brief was filed on concurrently herewith.